LISTING OF CLAIMS:

1-14 (Canceled)

15. (Currently amended) A method of manufacturing a semiconductor device comprising:

forming a second conductivity type region in a semiconductor substrate having a principal surface of a first conductivity type by implanting impurities of a second conductivity type two or more times;

forming a first conductivity type region inside the island of said second conductivity type region, said first conductivity type region having a higher impurity concentration than said semiconductor substrate;

forming a trench in a depth direction of said semiconductor substrate by anisotropic etching;

forming a sacrificed oxide film on an inner wall surface of the trench by thermal oxidation;

removing said sacrificed oxide film;

forming an insulation film in an interior of said trench; ~~and~~

filling said trench formed said insulation film with a polycrystalline silicon ~~film~~film;

forming a plurality of electric field alleviating regions by introducing impurities of the second conductivity type in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region;

forming a plurality of strip-wise highly doped second conductivity type regions each formed inside each of the electric field alleviating regions;

forming a plurality of strip-wise third trenches each formed inside each of the strip-wise second conductivity type regions in a depth direction of said semiconductor substrate by anisotropic etching;

forming a plurality of deeper second conductivity type regions each formed inside each of said third trenches by introducing impurities of the second conductivity type by two or more ion implantation steps;

forming a metal electrode which electrically connects each of said strip-wise second conductivity type region to each of said deeper second conductivity type region; and

forming a protection film at least on a surface of the semiconductor substrate except a region where said second conductivity type region underlies.

16. (Original) The method of manufacturing a semiconductor device according to claim 15, further comprising, after the trench is filled with the polycrystalline silicon film:

patterning said film of polycrystalline silicon film so that the patterned polycrystalline silicon film has a T-shaped cross section with a wider width than an opening of said trench;

forming a highly doped first conductivity type region having a higher concentration than said first conductivity type region inside said first conductivity type region at a portion not coated by said polycrystalline silicon film; and

forming a highly doped second conductivity type layer region inside said first conductivity type region formed at a region enclosed by two of said trenches.

17. (Original) The method of manufacturing a semiconductor device according to claim 15, wherein, said second conductivity type region is formed by performing ion implantation two or more times, and the each ion implantation of the impurities of the second conductivity type is carried out under a condition that acceleration energy is 200 keV or higher.

18. (Canceled)

19. (Original) The method of manufacturing a semiconductor device according to claim 16, wherein said highly doped first conductivity type region is formed under a condition that a dose of implant ions is 1.0×10^{15} (atoms/cm^2) or less.

20. (Currently amended) A method of manufacturing a semiconductor device comprising:

forming a second conductivity type region in a semiconductor substrate having a principal surface of a first conductivity type;

forming a first conductivity type region inside said second conductivity type region, the first conductivity type region having a higher concentration than said semiconductor substrate;

forming a plurality of first trenches in a depth direction of said semiconductor substrate by anisotropic etching;

forming a sacrificed oxide film formed on an inner surface wall of each of the first trenches by thermal oxidation;

removing said sacrificed oxide film;

forming an insulation film in an interior of each of said first trenches;

filling each of the first trenches with a polycrystalline silicon film;

forming a plurality of second trenches in the second conductivity type region each positioned between an adjacent pair of said plurality of first trenches in parallel with said plurality of first trenches;

forming a second conductivity type protrusion region with a junction deeper than a junction of said second conductivity type region by introducing impurities of the second conductivity type from each of the second trenches by two or more ion implantation steps; and

forming a metal electrode so as to electrically connect said first conductivity type region with said second conductivity type protrusion region in each of the second ~~trenches~~trenches;

after each of the first trenches is filled with the polycrystalline silicon film,

patterning said polycrystalline silicon film so that the patterned polycrystalline silicon film has a T-shaped cross section with a wider width than an opening of each of the first trenches;

forming a highly doped first conductivity type region inside said first conductivity type region at a portion from which said polycrystalline silicon film is removed, said highly doped first conductivity type region having a higher concentration than said first conductivity type region; and

forming a highly doped second conductivity type layer region inside said highly doped first conductivity type region at a portion between an adjacent two of said plurality of first trenches.

21. (Canceled)

22. (Previously presented) The method of manufacturing a semiconductor device according to claim 20, wherein at least one of said ion implantation steps is carried out at acceleration energy of 200 keV or higher.

23. (Previously presented) The method of manufacturing a semiconductor device according to claim 20, wherein at least one of said ion implantation steps is carried out at acceleration energy of 30 keV or lower and a dose of implant ions at 1.0×10^{15} (atoms/cm^2) or more.

24. (Original) The method of manufacturing a semiconductor device according to claim 20, wherein the island of said second conductivity type region is formed by introducing impurities of a second conductivity type by two or more ion implantations.

25. (Canceled)

26. (Currently amended) A method of manufacturing a semiconductor device comprising:

forming a second conductivity type region in a semiconductor substrate having a principal surface of a first conductivity type;

forming a first conductivity type region inside said second conductivity type region, the first conductivity type region having a higher concentration than said semiconductor substrate;

forming a plurality of first trenches in a depth direction of said semiconductor substrate by anisotropic etching;

forming a sacrificed oxide film formed on an inner surface wall of each of the first trenches by thermal oxidation;

removing said sacrificed oxide film;

forming an insulation film in an interior of each of said first trenches;

filling each of the first trenches with a polycrystalline silicon film;

forming a plurality of second trenches in the second conductivity type region each positioned between an adjacent pair of said plurality of first trenches in parallel with said plurality of first trenches;

forming a second conductivity type protrusion region with a junction deeper than a junction of said second conductivity type region by introducing impurities of the second conductivity type from each of the second trenches by two or more ion implantation steps;

forming a metal electrode so as to electrically connect said first conductivity type region with said second conductivity type protrusion region in each of the second trenches;

~~The method of manufacturing a semiconductor device according to claim 20, further comprising:~~

forming a plurality of electric field alleviating regions by introducing impurities of the second conductivity type in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region;

forming a plurality of strip-wise highly doped second conductivity type regions each formed inside each of the electric field alleviating regions;

forming a plurality of strip-wise third trenches each formed inside each of the strip-wise second conductivity type regions in a depth direction of said semiconductor substrate by anisotropic etching;

forming a plurality of deeper second conductivity type regions each formed inside each of said third trenches by introducing impurities of the second conductivity type by two or more ion implantation steps;

forming a metal electrode which electrically connects each of said strip-wise second conductivity type region to each of said deeper second conductivity type region; and

forming a protection film at least on a surface of the semiconductor substrate except a region where said second conductivity type region underlies.

27. (Currently amended) The method of manufacturing a semiconductor device according to ~~claim 25~~claim 15, wherein each of said deeper second-conductivity type region has a junction deeper than a junction of said second conductivity type region for forming a channel in a gate driving type power element having a high voltage withstanding characteristics.

28. (Original) The method of manufacturing a semiconductor device according to claim 26, wherein each of said deeper second conductivity type region has a junction deeper than a junction of said second conductivity type region for forming a channel in a gate driving type power element having a high voltage withstanding characteristics.